XT1D104 Datasheet

Ver-1.1

General Description

The XT1D104 is a 4-output differential high performance clock buffer.

The input can be selected between two differential inputs or a singular crystal input. The selected input clock is then evenly distributed across two sets of differential outputs and a single LVCMOS output. These outputs can be set up with LVPECL, LVDS, or HCSL drivers according to necessity, or be turned off. The LVCMOS output is further equipped with a synchronous enable input, ensuring consistent operation without interruption by runt pulses, whether it is active or not. The output levels are predetermined and can remain stable even when the inputs are disconnected.

When the crystal input is not in use, the device's internal oscillator circuit is programmed to shut off automatically. The crystal connection is compatible with a single-ended clock signal.

The device is designed for a signal fan out of high frequency, low phase-noise clock. It is designed to operate from a 3.3V/2.5V core power supply, and 3 independent output supplies: 3.3V/2.5V.

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-gigabit ethernet, XAUI, SATA/SAS, SONET/SDH, CPRI, high frequency back planes
- Switches, routers, line Cards, timing cards
- Servers, computing, PCI express (PCIe 3.0, 4.0)
- Remote radio units and base band units
- Test and measurement

Features

- Two differential reference clock pairs
- Input pairs can accept the following differential input levels:

  LVPECL, LVDS, HCSL, HSTL or single ended
- Crystal Input accepts 10MHz to 100MHz Crystal or Single Ended Clock.

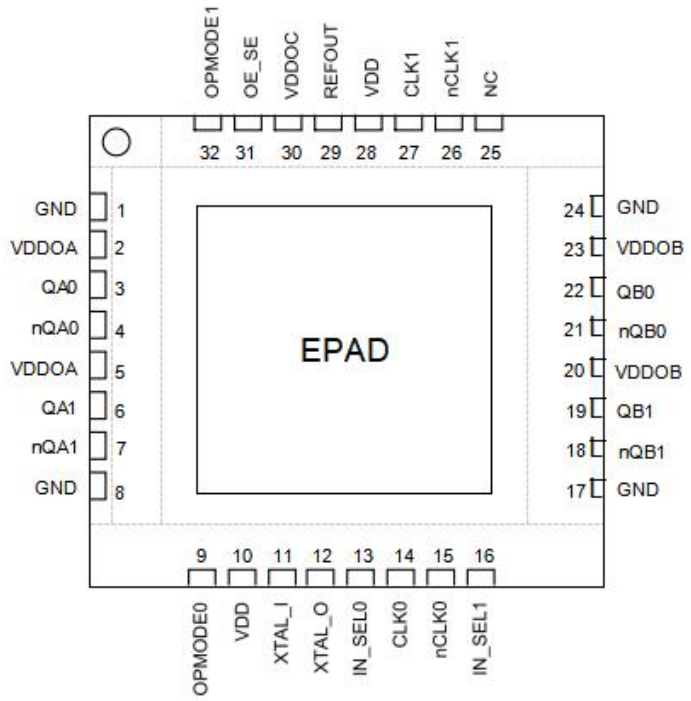
  Maximum output frequency

LVPECL	- 2GHz
LVDS	- 2GHz
HCSL	- 350MHz
LVCMOS	- 250MHz
- Two banks, each has five differential output pairs that can be separately configured as LVPECL or LVDS or HCSL or Hi-Z
- One single-ended reference output with synchronous enable to avoid glitch
- Output skew: 30ps (typical)
- Part-to-part skew: 60ps (typical)

  Additive RMS phase jitter @ 156.25MHz:
  50 fs RMS (10kHz - 20MHz), @ 3.3V/ 3.3V
- Supply voltage modes:

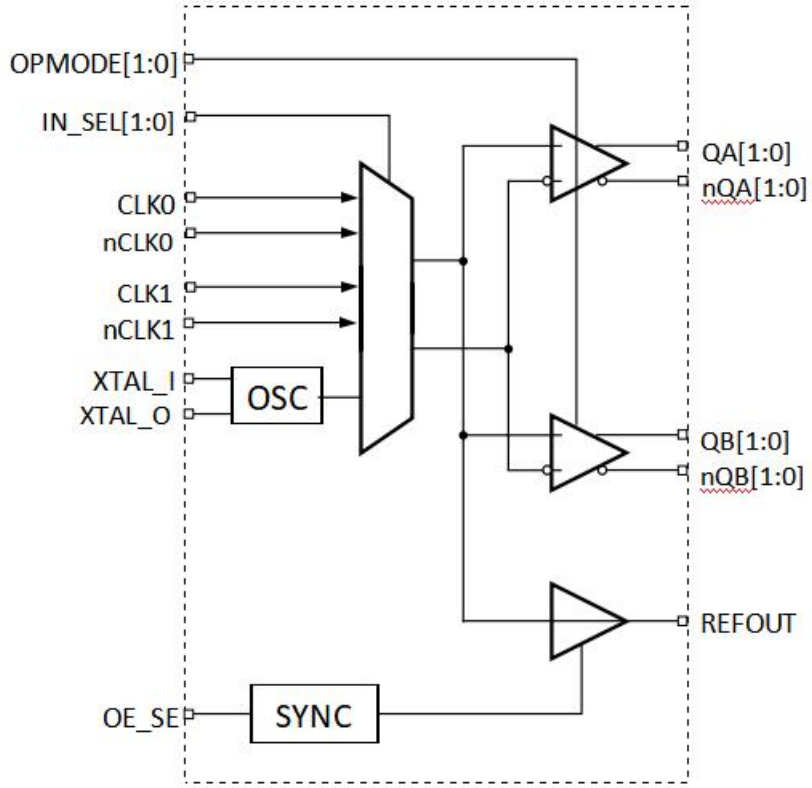
VDD	VDDO
3.3V	3.3V
3.3V	2.5V
2.5V	2.5V
- Operation temperature range: -40°C to 85°C:
- Package: 32-pin, 5mm*5mm QFN

Pin Configuration：



32-pin QFN (Top View)

Block Diagram：



Pin Descriptions：

Number	Name	Type		Description
1	GND	Power		Ground.
2	VDDOA	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
3	QA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
4	nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5	VDDOA	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
6	QA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
7	nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
8	GND	Power		Ground.
9	OPMODE0	Input	Pulldown	Output driver select for Bank A outputs. LVCMOS/LVTTL interface levels.
10	VDD	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
11	XTAL_I	Input		Crystal oscillator interface.
12	XTAL_O	Input		Crystal oscillator interface.
13	IN_SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels.
14	CLK0	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
15	nCLK0	Input	Pullup/Pulldown	Inverting differential clock. Internally biased to 0.5VDD.
16	IN_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels.
17	GND	Power		Ground.
18	nQB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
19	QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
20	VDDOB	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
21	nQB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
22	QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
23	VDDOB	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
24	GND	Power		Ground.
25	NC	Unused		NC
26	nCLK1	Input	Pullup/Pulldown	Inverting differential clock. Internally biased to 0.5VDD.
27	CLK1	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
28	VDD	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
29	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
30	VDDOC	Power		Output supply pin for REFOUT output.
31	OE_SE	Input	Pulldown	REFOUT output enable. LVCMOS/LVTTL interface levels.
32	OPMODE1	Input	Pulldown	Output driver select for Bank A outputs. LVCMOS/LVTTL interface levels.